Study of FinFET Based SRAM Cells

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***Abstract*-- This presents the transistors have been shrinking exponentially size and therefore the transistors in a single microelectronic chip have been rising exponentially. In the current generation of transistors, the exponential reduce in transistor size can continue. This generation is multi gate transistors. Fin FETs are the most appealing option due to their better scalability and options for advance SRAM performance. Fin FET based 6T SRAM cells manufactured with pass gate feedback attain significant developments in the cell read stability without area penalty. The write ability can be improved on the use of pull up writing gating with a separate write word line. In 9T SRAM cell, an appropriate read operation is given by overpowering the drain induced barrier lowering effect and controlling the body source voltage change.**

***Keywords*- FinFET, FinFET structure, SRAM, multi gate transistor, 6T SRAM cell, SRAM read/write margin. 9T SRAM Cell, performance enhancement techniques.**

1. INTRODUCTION

FinFET:

FinFET is a field effect transistor device structure and towards for forming FETs for scaled semiconductor devices. FinFET, a multi gate transistor is a promising technology for make bigger Moore's Law. FinFET are designed to reduce Short Channel Effects(SCE), various leakage currents and sizing of Planner FETs. Double gates are provided with the part of the channel to provide enhanced drive current and effectively hold back short channel effects a plurality of channels can be provided for creating current capacity.

In one embodiment, a Fin FET device for characterization incorporates an active fin including a source fin, a depletions fin, and a drain fin; a edge fin prolonging from the depletion fin and combined to a body contact for providing access for device description .A fin FET device is made using a conventional MOSFET technology. The firstly made fin field-effect transistor (FinFET)-similar silicon-on-insulator (SOI) MOS device dates to bring up to 1989, which is be familiar with as the completely reduced lean-channel transistor with a silicon films ranking perpendicularly. With the incessant scaling of MOS design into the 45-nm technology lump, nonplanar dual-gate (DG) MOSFETs (like FinFETs) have become appealing to their good restrain of short channel effects, ideal sub threshold slope, and high current drive.

FEATURES :

FinFET made up of a vertical Si fin which was controlled by self aligned double gate.

Main feature of FinFET:

- Ultra thin Si for suppression of short channel effects
- Increase source/drain voltage to reduce parasitic resistance and improve current drives
- It gives us the last process of low T, high k gate dielectric
- Symmetric gates give great performance, but it can be built asymmetric gates that target will be VT.

FinFET Structures

There are two types:-

- Shorted Gate FinFET: In shorted Gate FinFETs the two gates are correlated together, leading to a three terminal device.This can assist as a direct replacement of the conventional bulk CMOS devices.
- Independent Gate FinFET: In self governing Gate FinFET, the top part of the gate is engraved out, giving method to two self sufficient gates. Because the two self sufficient gates can be controlled separately, IG mode FinFET offer more design options.

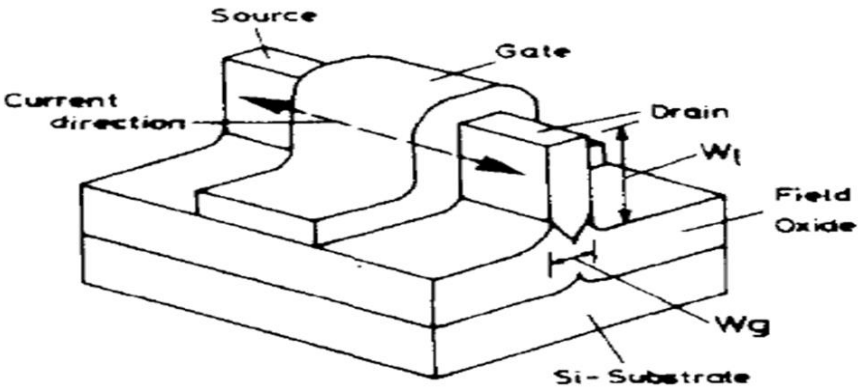

Fig.1 FirstFinFET DELTA(Depleted Lean channels Transistor)[1]

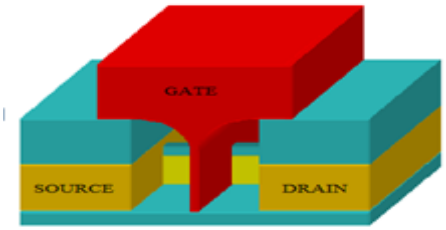

Fig.2 Original: Gate-last process flow[1]

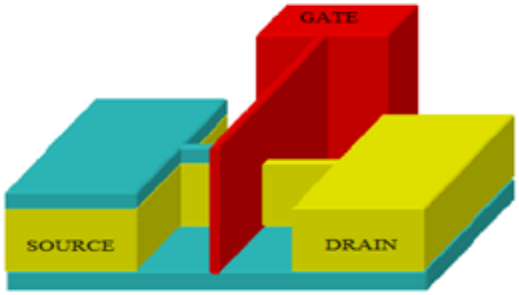

Fig.3 Improved: Gate-first process flow[1]

SRAM

- SRAM is a volatile memory and is used to store most of the data but the difficulty is that the SRAM cell needs continuous power.
- SRAM cell has three form into operation: read, write and hold.
- SRAM has more power dissipation due to hold data the static power are needed to keep the SRAM cell in ON condition.
- SRAMs main benefit is fast accessing its data and reliability.

2. LITERATURE SURVEY

MULTIGATE TRANSISTOR [1]:

This paper presented that for more than four decades, transistors have been get smaller exponentially in size, and so the number of transistors in a single microelectronic chip has been rising exponentially. Such as rise in packing thickness was made possible by continually cowering the MOSFET. In the present production of transistors, the transistor measurements have shrunk to such an extent that the electrical typical of the device can be markedly degraded, making it unlikely that the exponential reduce in

transistor size can continue. Recently, however, an another generation of MOSFETs, called multi gate transistors, has come out, and this multi gate geometry will allow the remain improvement of computer performance into the next decade. a. Two n type regions called the source and the drain is formed into a p-type substrate. b. The width of the drain junction depletions region increases as the drain voltage increases, causing the drain-induced barrier lowering effect.[2]

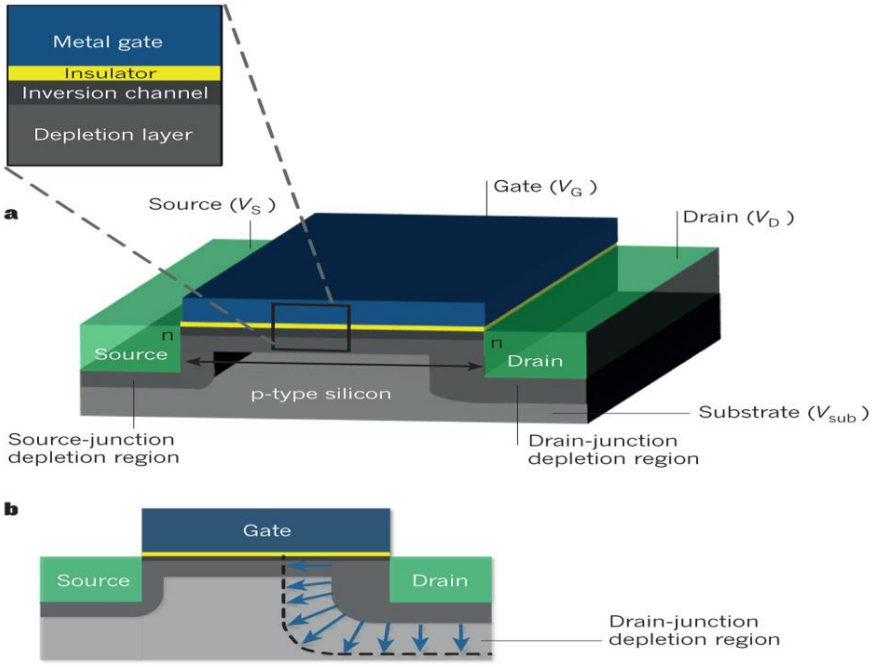

Fig. 4 A Schematic belief of a classical bulk n channels MOSFET[2].

6T SRAM Cell [3]

SRAM has become a main component in many VLSI Chipses because of their large storage density and small access period. SRAM has become the topic of considerable research due to the fast development for less power, low voltage memory design during recent years due to rise demand for laptops, IC memory cards and hand held contact devices. SRAMs are wide used for mobile applications both on chip as well as off chip memories, due to their get better of use and low standby leakage. The main objective is evaluating performance in terms of Power use, delay and Static Noise Margin of existing 6T CMOS SRAM cell in 45nm and 180nm technology [3].

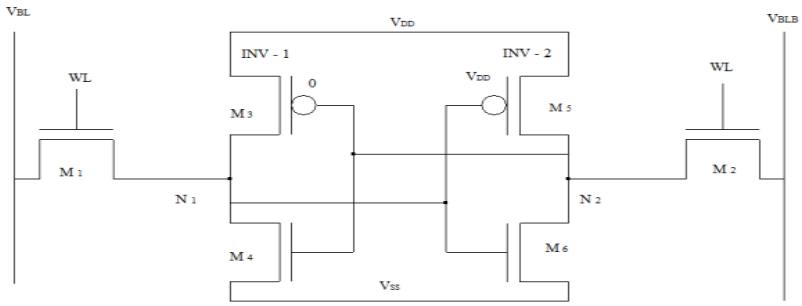

Fig.No.5 Schematic diagram of a standard 6T SRAM[3]

SRAM Read/Write Margin[4]:

The process-induced variants and sub-threshold leakage of bulk-Si technology boundary the extent of SRAM into sub-32 nm nodes. New design architectures are being thought about to get well control and decrease short channel effects. Among the probable candidates, FinFETs are the most appealing option because of their good scalability and possibilities for advance SRAM performance and produce enhancement through separate gating. It is shown that FinFET-based 6-T SRAM cells considered with pass-gate feedback (PGFB) attain significant improvements in the cell read steadiness exclusive of area penalty. The write-ability of the cell was able to get well through the help of pull-up write gating (PUWG) with a share write word line (WWL). The benefits of these two methods are complementary and additive, allowing for simultaneous read and write to create enhancements when the PGFB and PUWG designs are used in mixture.[4]

9T SRAM Cell [5]:

A new nine-transistor (9T) SRAM cell manage in the subthreshold area. In the proposed 9T SRAM cell, a proper read operationis provided by hold back the drain-induced barrier lowering effect and contain the body–source voltage dynamically. In the suggest cell, a common bit-line is usedin the read and write operations. This arrange leads to a larger write margin without using extra circuits.

The proposed 9T SRAM attains the contributions shown below:

- Static power reduction because of M7 and M8 by using lively controlled source-body voltage and suppressed DIBL effect
- Read access time reduction by utilizing L-Vt transistors and suitable at ULV
- The WM development of the SRAM cell
- Low Energy used
- PVT variation reduction.[5]

A survey on the performance analysis of FinFET Cells for various technologies. Industry requires excessive functioning trough power devices and memories. CMOS devices are scaled out to decrease the size. Therefore, As CMOS devices get scaled down the changes in the configuration metrics like SNM, Leakage power and delay get rise. FinFET become an essential technology in the VLSI design to overcome the short comes of CMOS. from recent years, FinFET has become the well promising alternative of conventional CMOS, IG, TG. FinFET SRAM standard cells functioning analysis has been carried out with respect to leakage power, SNM and delay [6].

Table 1 Summary of techniques for design enhancement of FinFET SRAM

Authors	Technique	Advantage	Disadvantage
M.Parimaladevi, D.Sharmilab, L.Kowsikaa	Theoretical studied of SRAM	Simple description of FinFET	Doesn't specifically highlight the best solution
P. Zhang , D. Connelly.	SRAM with 6T, FinFET	Saving of 20% of cell area	Study lacks benchmarking
J.H .Lee	14nm, Bulk & SOI FinFET	325K of temperature reduction	-No Benchmarking
M.Ansari, H.A.Kusha, B.Ebrahimi	7T SRAM	Highly stable, 57% of reduced power consumption	-No Design optimization
H.Farkhani, A.Periavi, F Moradi	10T SRAM	-33% minimization of leakage power	-Less Effective benchmarking
A.Shafaei, S.Chen, Y.Wang	6T, 8T SRAM with 7nm FinFET , cross layer	-memory efficient memory	-No variability analysis considered.

CONCLUSION

In this paper, operative techniques based on dynamically containing source body voltage and DIBL achieve for the readout path transistor and also a packed pMOS device were utilized in order to decrease the power use in the hold state and get better the presentation of the read operation. As we scale down from micro meter to nano meter the short channel effects happen which causes leakage currents etc to reduce these we attempt from planner MOS to FinFET which is MUGFET.

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